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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,982	12/30/2003	Kei-Kang Hung	JLINP093.DIV3	9700

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,982	HUNG ET AL	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a channel length of each of said MOS transistors in said second MOS transistor array is larger than that of each of said MOS transistors in said first MOS transistor array, as recited in claim 1, are unclear as to whether the term larger means that the channel length of each of said MOS transistors in said second MOS transistor array is longer, wider, deeper or have larger volume than that of the first MOS transistor array.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3-4, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (6,445,215) or Wollesen (5,828,110) in view of Ker et al. (5,852,315).

Takahashi et al. teach in figure 1 and related text a semiconductor device comprising

a first MOS transistor array M23, M24 (p-MOS) formed in a region and having a plurality of MOS transistors;

a second MOS transistor array M21, M22 (n-MOS) formed in a region and having a plurality of MOS transistors, wherein a channel length of each of said MOS transistors in said second MOS transistor array is larger than that of each of said MOS transistors in said first MOS transistor array (column 2, lines 37-42).

Takahashi et al. do not teach first and second MOS transistor arrays with ESD protective combination surrounded by first and second guard rings, respectively.

Wollesen teach in figure 11 and related text a semiconductor device with ESD protective combination comprising

a first guard ring 114;

a first MOS transistor array 110 formed in a region surrounded by said first guard ring;

a second guard ring 102 adjacent to said first guard ring; and

a second MOS transistor array 100 formed in a region surrounded by said second guard ring, wherein a channel length (the area under the gate electrode) of each

of said MOS transistors in said second MOS transistor array is larger than that of each of said MOS transistors in said first MOS transistor array (as depicted in figure 11). Wollesen does not teach a plurality of MOS transistors.

Ker et al. teach in figure 8 and related text first (p-MOS) and second (n-MOS) MOS transistor arrays comprising a plurality of MOS transistors and surrounded by first and second guard rings, respectively, which can be used with ESD protective combination (column 1, lines 27-31). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to surround Takahashi et al.'s p-MOS and n-MOS transistors with first and second guard rings, and to form Wollesen's n-MOS and p-MOS transistors as a plurality of MOS transistors with ESD protective combination, as taught by Ker et al., in order to improve the device characteristics by providing better protection for the device, and in order to use the device in a practical application which requires plurality of transistors, respectively.

Regarding the claimed limitations of a semiconductor device with ESD protective combination, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Furthermore, the recitation of a semiconductor device with ESD protective combination occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claims 3-4, Takahashi et al. and Wollesen teach gates of said MOS transistors in said first MOS transistor array are electrically connected to each other, and gates of said MOS transistors in said second MOS transistor array are electrically connected to each other, wherein gates of said MOS transistors in said first MOS transistor array are grounded, and gates of said MOS transistors in said second MOS transistor array are grounded.

Claim 2, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al., Wollesen and Ker et al., as applied to claim 1 above, and further in view of Applicant Admitted Prior Art (AAPA). Takahashi et al., Wollesen and Ker et al. teach substantially the entire claimed structure, as applied to claim 1 above, except first and second isolation portions formed between said first guard ring and said first MOS transistor array, and between said second guard ring and said second MOS transistor array, respectively.

AAPA teaches in figure 1A an isolation portion formed between the guard ring 11 and the MOS transistor array. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first and second isolation portions between said first guard ring and said first MOS transistor array, and between said second guard ring and said second MOS transistor array, respectively, in the devices of Takahashi et al., Wollesen and Ker et al., in order to improve the device characteristics by providing better protection for the device.

Response to Arguments

Applicant argues that Wollesen and Takahashi et al. do not teach an ESD device.

Wollesen teaches a semiconductor device with ESD protective combination (see column 3, lines 3-7). Regarding the claimed limitations of a semiconductor device with ESD protective combination, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Furthermore, the recitation of a semiconductor device with ESD protective combination occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Applicant argues that Wollesen does not teach in figure 11 a channel length of each of said MOS transistors in said second MOS transistor array is larger than that of each of said MOS transistors in said first MOS transistor array, because figure 11 is an inaccurate figure and was provided just for the illustration of the invention layout.

Figure 11 depicts a channel length (the area under the gate electrode) of each of said MOS transistors in said second MOS transistor array is larger than that of each of said MOS transistors in said first MOS transistor array. Although the disclosure does not mention that the channel length of each of said MOS transistors in said second MOS transistor array is larger than that of each of said MOS transistors in said first MOS transistor array, an artisan forming Wollesen's device would not be motivated to deviate from Wollesen's teaching in figure 11 to form two identical channel lengths, but would rather form MOS transistors comprising channels as depicted in figure 11.

Applicant argues that it is impossible for Wollesen to teach the gates of the first and second MOS transistors are electrically connected, because Wollesen teaches only a p MOS and an n MOS.

Wollesen teaches a CMOS device. It is well known that the gates of the first and second MOS transistors of a CMOS device are electrically connected. Therefore, Wollesen teaches the gates of the first and second MOS transistors are electrically connected, as claimed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
12/28/04

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800